Experiment #4
CMOS 4046 Phase-Locked Loop

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The purpose of this lab assignment is to introduce operating principles and characteristics of a phase-locked loop (PLL) built around CMOS 4046 integrated circuit.

In the lab assignment #5, this PLL will be used to design a data modem based on a digital frequency modulation technique called frequency-shift keying (FSK). Before approaching the design problem, it is necessary to understand principles of operation and characteristics of the PLL.

This handout includes: a brief summary of the theory of phase-locked loops in Section 1, description of the PLL components on the 4046 chip in Section 2, experiments you need to perform in the lab in Section 3, and the prelab assignment in Section 4.

1 Phase-Locked Loop Concepts

Phase-locked loop is a feedback loop where a voltage-controlled oscillator can be automatically synchronized ("locked") to a periodic input signal. The locking property of the PLL has numerous applications in communication systems (such as frequency, amplitude, or phase modulation/demodulation, analog or digital), tone decoding, clock and data recovery, self-tunable filters, frequency synthesis, motor speed control, etc.

The basic PLL has three components connected in a feedback loop, as shown in the block diagram of Fig. 1: a voltage-controlled oscillator (VCO), a phase detector (PD), and a low-pass loop filter (LPF).

The VCO is an oscillator whose frequency f_{osc} is proportional to input voltage v_o. The voltage at the input of the VCO determines the frequency f_{osc} of the periodic signal v_{osc} at the output of the VCO. In the lab #3 you have designed one VCO.

The output of the VCO, v_{osc}, and a periodic incoming signal v_i are inputs to the *phase detector*. When the loop is *locked* on the incoming signal v_i, the frequency f_{osc} of the VCO output v_{osc} is *exactly equal* to the frequency f_i of the periodic signal v_i,

$$f_{osc} = f_i \,. \tag{1}$$

It is also said that the PLL is in the *locked condition*. The phase detector produces a signal proportional to the phase difference between the incoming signal and the VCO output signal.

The output of the phase detector is filtered by a low-pass *loop filter*. The loop is closed by connecting the filter output to the input of the VCO. Therefore, the filter output voltage v_o controls the frequency of the VCO.

A basic property of the PLL is that it attempts to maintain the frequency lock ($f_{osc} = f_i$) between v_{osc} and v_i even if the frequency f_i of the incoming signal varies in time. Suppose that the PLL is in the locked condition, and that the frequency f_i of the incoming signal increases slightly. The phase difference between the VCO signal and the incoming signal will begin to increase in time.

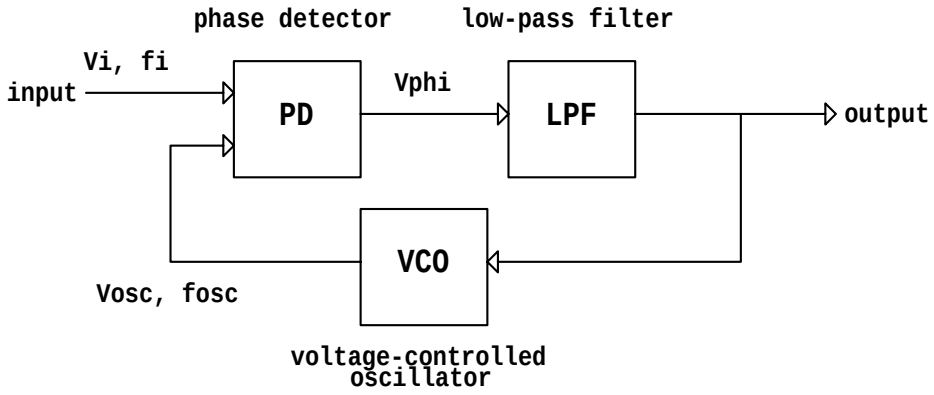

Figure 1: Block diagram of a basic phase-locked loop (PLL).

As a result, the filter output voltage v_o increases, and the VCO output frequency f_{osc} increases until it matches f_i, thus keeping the PLL in the locked condition.

The range of frequencies from $f_i = f_{min}$ to $f_i = f_{max}$ where the locked PLL *remains* in the locked condition is called the *lock range* of the PLL. If the PLL is initially locked, and f_i becomes smaller than f_{min}, or if f_i exceeds f_{max}, the PLL fails to keep f_{osc} equal to f_i, and the PLL becomes unlocked, $f_{osc} \neq f_i$. When the PLL is unlocked, the VCO oscillates at the frequency f_o called the *center* frequency, or the *free-running* frequency of the VCO. The lock can be established again if the incoming signal frequency f_i gets close enough to f_o. The range of frequencies $f_i = f_o - f_c$ to $f_i = f_o + f_c$ such that the initially unlocked PLL becomes locked is called the *capture range* of the PLL.

The lock range is wider than the capture range. So, if the VCO output frequency f_{osc} is plotted against the incoming frequency f_i, we obtain the PLL steady-state characteristic shown in Fig. 2. The characteristic simply shows that $f_{osc} = f_i$ in the locked condition, and that $f_{osc} = f_o = const.$ when the PLL is unlocked. A hysteresis can be observed in the $f_{osc}(f_i)$ characteristic because the capture range is smaller than the lock range.

We can now examine how the PLL is actually implemented on the CMOS 4046 integrated circuit.

2 The 4046 Phase-Locked Loop

A diagram of the 4046 PLL is shown in Fig. 3.

A single positive supply voltage is needed for the chip. The positive supply voltage V_{DD} is connected to pin 16 and the ground is connected to pin 8. In the lab we will use $+V_{DD} = +15$V.

The incoming signal v_i goes to the input of an internal amplifier at the pin 14 of the chip. The internal amplifier has the input biased at about $+V_{DD}/2$. Therefore, the incoming signal can be capacitively coupled to the input, as shown in Fig. 3. The incoming ac signal v_i of about one volt peak-to-peak is sufficient for proper operation. The capacitor C_i together with the input resistance $R_i \approx 100k\Omega$ at the pin 14 form a high-pass filter. C_i should be selected so that v_i is in the pass-

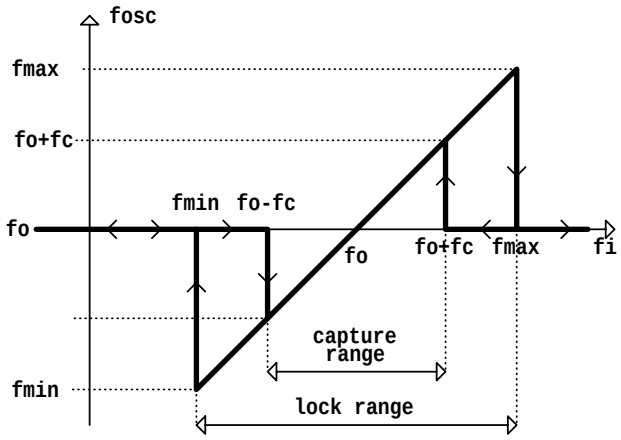

Figure 2: Steady-state $f_{osc}(f_i)$ characteristic of the basic PLL.

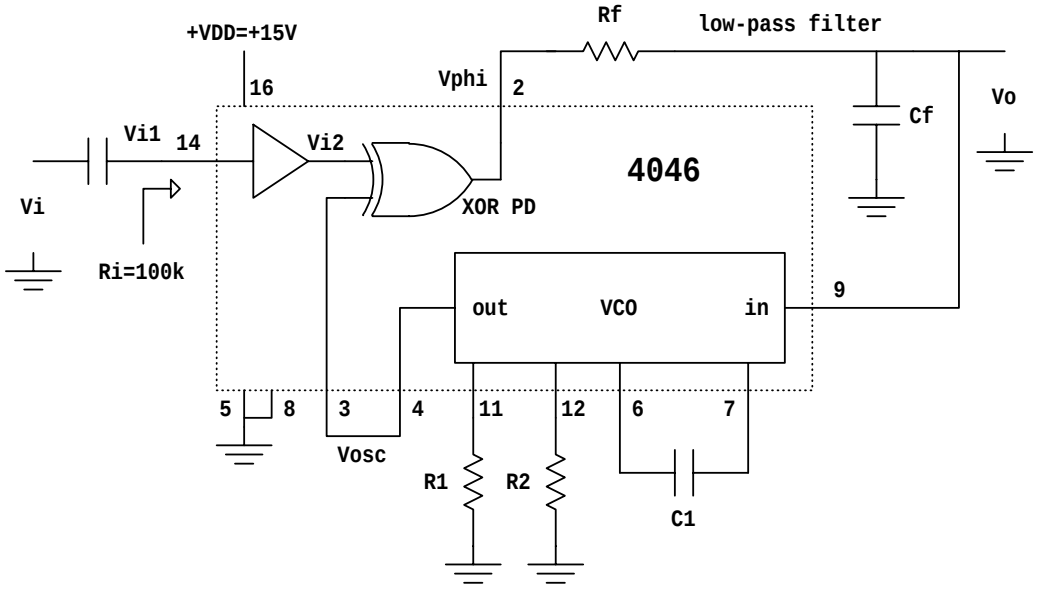

Figure 3: CMOS 4046 PLL: basic connection diagram.

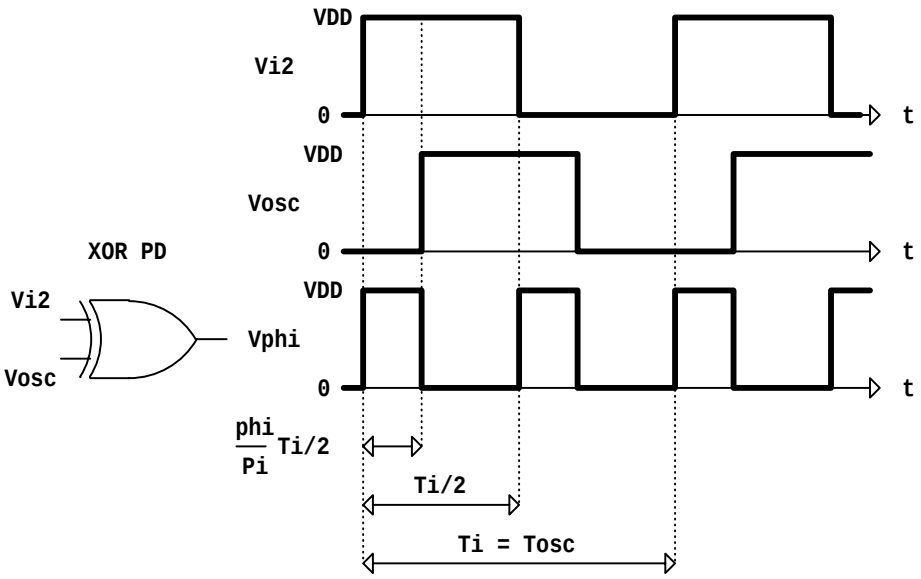

Figure 4: Operation of the phase detector with XOR gate.

band of the filter, i.e., so that $f_i > 1/(2\pi R_i C_i)$ for the lowest expected frequency f_i of the incoming signal. The output v_1 of the internal amplifier is internally connected to one of the two inputs of the phase detector on the chip.

2.1 Phase Detector

The phase detector on the 4046 is simply an XOR logic gate, with logic low output ($v_\phi = 0$V) when the two inputs are both high or both low, and the logic high output ($v_\phi = V_{DD}$) otherwise. Fig. 4 illustrates the operation of the XOR phase detector when the PLL is in the locked condition. v_1 (the amplified v_i) and v_{osc} (the VCO output) are two phase-shifted periodic square-wave signals at the same frequency $f_{osc} = f_i = 1/T_i$, and with 50% duty ratios. The output of the phase detector is a periodic square-wave signal $v_\phi(t)$ at the frequency $2f_i$, and with the duty ratio D_ϕ that depends on the phase difference ϕ between v_i and v_{osc},

$$D_\phi = \frac{\phi}{\pi}\,. \tag{2}$$

The periodic signal $v_\phi(t)$ at the output of the XOR phase detector can be written as the Fourier series:

$$v_\phi(t) = v_o + \sum_{k=1}^{k\to\infty} v_k \sin((4k\pi f_i)t - \theta_k)\,, \tag{3}$$

where v_o is the dc component of $v_\phi(t)$, and v_k is the amplitude of the k^{th} harmonic at the frequency $2kf_i$. The dc component of the phase detector output can be found easily as the average of $v_\phi(t)$

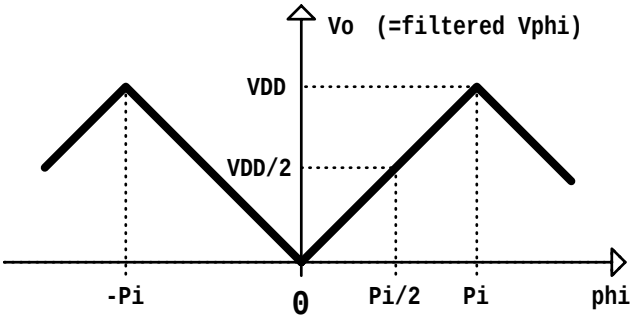

Figure 5: Characteristic of the phase detector.

over a period $T_i/2$,

$$v_o = \frac{1}{T_i/2}\int_0^{T_i/2} v_\phi(t)dt = \frac{2}{T_i}\int_0^{D_\phi T_i/2} V_{DD}dt = \frac{V_{DD}}{\pi}\phi. \tag{4}$$

2.2 Loop Filter

The output v_ϕ of the phase detector is filtered by an external low-pass filter. In Fig. 3, the loop filter is a simple passive RC filter. The purpose of the low-pass filter is to pass the dc and low-frequency portions of $v_\phi(t)$ and to attenuate high-frequency ac components at frequencies $2kf_i$. The simple RC filter has the transfer function:

$$F(s) = \frac{1}{1+sR_fC_f} = \frac{1}{1+s/w_p}, \tag{5}$$

where

$$f_p = \frac{w_p}{2\pi} = \frac{1}{2\pi R_fC_f} \tag{6}$$

is the cut-off frequency of the filter. If $f_p << 2f_i$, i.e., if the cut-off frequency of the filter is much smaller than twice the frequency f_i of the incoming signal, the output of the filter is approximately equal to the dc component v_o of the phase detector output. In practice, the high-frequency components are not completely eliminated and can be observed as high-frequency ac ripple around the dc or slowly-varying v_o.

Eq. 4 shows that v_o is proportional to the phase difference ϕ between the incoming signal $v_i(t)$ and the signal $v_{osc}(t)$ from the VCO. The constant of proportionality,

$$K_D = \frac{V_{DD}}{\pi} \tag{7}$$

is called the *gain or the sensitivity* of the phase detector. This expression is valid for $0 \le \phi \le \pi$. In general, the filter output v_o as a function of the phase difference ϕ is shown in Fig. 5. Note that $v_o = 0$ if v_i and v_{osc} are in phase ($\phi = 0$), and that it reaches the maximum value $v_o = V_{DD}$ when

the two signals are exactly out of phase ($\phi = \pi$). From Fig. 4 it is easy to see that for $\phi < 0$, v_o increases, and for $\phi > \pi$, v_o decreases. Of course, the characteristic is periodic in ϕ with period 2π. The range $0 \leq \phi \leq \pi$ is the range where the PLL can operate in the locked condition.

2.3 Voltage Controlled Oscillator

As shown in Fig. 3, the filter output v_o controls the VCO, i.e., determines the frequency f_{osc} of the VCO output v_{osc}. The VCO inside the 4046 chip is based on the same operating principles as the VCO you built in the lab #3. The voltage v_o controls the charging and discharging currents through an external capacitor C_1, and therefore determines the time needed to charge (discharge) the capacitor to a pre-determined threshold level. As a result, the frequency f_{osc} of the VCO output is determined by v_o. The VCO output v_{osc} is a square wave with 50% duty ratio and frequency f_{osc}.

As shown in Fig. 3, the VCO characteristics are user-adjustable by three external components: R_1, R_2 and C_1. When v_o is at zero, the VCO operates at the minimum frequency f_{min} given approximately by:

$$f_{min} = \frac{1}{R_2(C_1 + 32pF)}\,. \tag{8}$$

When $v_o = V_{DD}$, the VCO operates at the maximum frequency f_{max} given approximately by

$$f_{max} = f_{min} + \frac{1}{R_1(C_1 + 32pF)}\,. \tag{9}$$

Unfortunatelly, the actual operating frequencies can differ significantly from the values prediced by the above equations. As a result, you may need to tune the component values by experiment.

For proper operation of the VCO, the components R_1, R_2 and C_1 should satisfy:

$$1M\Omega \geq R_1 \geq 10k\Omega, \quad 1M\Omega \geq R_2 \geq 10k\Omega, \quad 100nF \geq C_1 \geq 100pF\,. \tag{10}$$

For f_{osc} between the minimum f_{min} and the maximum f_{max}, the VCO output frequency f_{osc} is ideally a linear function of the control voltage v_o. The slope $K_o = \Delta f_{osc}/\Delta v_o$ of the $f_{osc}(v_o)$ characteristic is called the *gain or the frequency sensitivity* of the VCO, in Hz/V.

Operation of the 4046 PLL can now be summarized as follows. Suppose that initially there is no incoming signal at all, $v_i = 0$. The VCO output v_{osc} is a square-wave signal with 50% duty ratio. Since $v_i = 0$ by assumption, the output of the XOR phase detector is exactly the same as the VCO output, $v_\phi = v_{osc}$. The low-pass filter attenuates ac components of v_ϕ so that the filter output is approximately equal to the dc component of v_ϕ. In this case, the dc component v_o is equal to $V_{DD}/2$ because v_ϕ is V_{DD} for one half of the period and 0 for the other half of the period. The filter output voltage v_o is the input of the VCO. Therefore, we conclude that the VCO operates at the frequency that corresponds to the voltage $v_o = +V_{DD}/2$ at the VCO input. This frequency is called the *center*, or the *free-running* frequency $f_{osc} = f_o$ of the PLL.

Suppose now that the incoming signal v_i at frequency f_i is brought to the input of the PLL, i.e., to one of the two inputs of the XOR phase detector. If the frequency f_i is sufficiently close to the free-running frequency f_o, the PLL will "capture" the incoming signal. During the capture process, the phase difference between v_i and v_{osc} changes in time, and therefore v_o changes in time until v_o reaches the value required to lock the VCO frequency f_{osc} to the frequency f_i of the incoming signal. In the locked condition $f_{osc} = f_i$, and v_i and v_{osc} are phase shifted by ϕ. The

phase difference ϕ between v_i and v_{osc} depends on the value of the incoming signal frequency f_i. If $f_i = f_o$, the phase difference must be exactly $\phi = \pi/2$ so that, from Eq. 4, $v_o = V_{DD}/2$ and the VCO indeed operates at f_o. If, for example, $f_i = f_{max}$, the phase difference ϕ must be equal to π in order to obtain $v_o = V_{DD}$ that results in the VCO output frequency equal to f_{max}. It is important to note here that in order to keep $f_{osc} = f_i$ in the locked condition, the filter output voltage v_o must vary together with the frequency f_i of the incoming signal. Therefore, a change in f_i causes a proportional change in v_o, as long as the PLL stays in the locked condition with $f_{osc} = f_i$. As a result, if the incoming signal is frequency modulated, with $f_i(t)$ varying in time, the PLL behaves as an FM demodulator with v_o as the demodulated output.

2.4 Lock and Capture Ranges

Once the PLL is in the locked condition, it remains locked as long as the VCO output frequency f_{osc} can be adjusted to match the incoming signal frequency f_i, i.e., as long as $f_{min} \leq f_i \leq f_{max}$. When the lock is lost, the VCO operates at the free-running frequency f_o, which is between f_{min} and f_{max}. To establish the lock again, i.e. to *capture* the incoming signal again, the incoming signal frequency f_i must be close enough to f_o. Here "close enough" means that f_i must be in the range from $f_o - f_c$ to $f_o + f_c$, where $2f_c$ is called the capture range. The capture range $2f_c$ is an important PLL parameter because it determines whether the locked condition can be established or not. Refer again to Fig. 2 that shows a typical steady-state PLL characteristic. Note that the capture range $2f_c$ is smaller than the lock range $f_{max} - f_{min}$.

The capture range $2f_c$ depends on the characteristics of the loop filter. For the simple RC filter, a very crude, approximate implicit expression for the capture range can be found as:

$$f_c \approx \frac{V_{DD}}{2} \frac{K_o}{\sqrt{1 + (f_c/f_p)^2}}, \tag{11}$$

where f_p is the cut-off frequency of the filter, V_{DD} is the supply voltage, and K_o is the VCO gain. Given K_o, and f_p, this relation can be solved for f_c numerically, which yields an approximate theoretical prediction for the capture range $2f_c$.

If the capture range is much larger than the cut-off frequency of the filter, $f_c/f_p >> 1$, the expression for the capture range is simplified,

$$2f_c \approx \sqrt{2K_o f_p V_{DD}}. \tag{12}$$

Note that the capture range $2f_c$ is smaller if the cut-off frequency f_p of the filter is lower. It is usually desirable to have a wider capture range, which can be accomplished by increasing the cut-off frequency f_p of the filter. On the other hand, a lower cut-off frequency f_p is desirable in order to better attenuate high-frequency components of v_ϕ at the phase detector output, and improve noise rejection in general. In Lab #5, we will discuss other aspects of the filter design in more details.

3 Experiments

The purpose of the lab experiments is to verify the basic PLL operation in practice and to determine or experimentally confirm the 4046 PLL characteristics needed for the design in Lab #5.

3.1 VCO Component Selection

The theoretical expressions for the VCO minimum frequency f_{min} and the maximum frequency f_{max} are unfortunately not very reliable. Experimentally determine R_1, R_2 and C_1 so that $f_{min} = 8$kHz and $f_{max} = 12$kHz. To adjust for f_{min} you can simply connect the VCO input (pin 9) to ground. To adjust for f_{max}, you can connect the pin 9 to V_{DD}. The loop filter is not needed in this part.

From the experiment, determine factors k_1 and k_2 in

$$f_{min} = \frac{k_1}{R_2(C_1 + 32pF)}\,, \tag{13}$$

$$f_{max} = f_{min} + \frac{k_2}{R_1(C_1 + 32pF)}\,, \tag{14}$$

so that the modified expressions can be used to estimate the required parameter values more accurately for a different set of specifications.

3.2 VCO Characteristics

Measure and plot the VCO characteristic $f_{osc}(v_o)$ for $0 \le v_o \le V_{DD}$. The loop filter is not needed in this part.

In the range $(v_o)_{min} \le v_o \le V_{DD}$, the VCO output frequency f_{osc} should change as a linear function of v_o. For $v_o < (v_o)_{min}$, the frequency f_{osc} does not depend on v_o.

Determine:

1. $(v_o)_{min}$,
2. the free-running VCO frequency f_o for $v_o = V_{DD}/2$, and
3. the gain K_o of the VCO.

If the VCO characteristic is linear, K_o can be determined from the end-points of the linear range,

$$K_o = \frac{f_{max} - f_{min}}{V_{DD} - (v_o)_{min}}\,. \tag{15}$$

Slope of a straight-line interpolation through the measured points for $v_o \ge (v_o)_{min}$ should give the same result.

3.3 Operation of the PLL

In this part you should close the loop by inserting the RC filter between the phase detector output and the VCO input, as shown in Fig. 3. Use a laboratory pulse generator as the source of the incoming signal v_i. Adjust frequency f_i of v_i to approximately match the free-running frequency f_o of the VCO. When v_i is applied, the PLL should operate in the locked condition, with f_{osc} exactly equal to f_i. The locked condition can be easily verified by observing v_i and v_{osc} *simultaneously* on a dual-trace oscilloscope. If $f_i = f_{osc}$, stable waveforms of *both* v_i and v_{osc} can be observed. Otherwise, one of the waveforms on the scope screen is blurred or is moving with respect to the other.

By changing f_i of the incoming signal, determine the actual lock range of the PLL, i.e., determine the maximum and the minimum frequency f_i such that starting from the locked condition the PLL remains in the locked condition. The lock range should be equal to $f_{max} - f_{min}$.

Determine the minimum peak-to-peak amplitude of the incoming signal v_i such that the PLL remains locked.

Get a hard copy or sketch the waveforms v_i, v_{osc} and v_ϕ for the PLL in the locked condition, at three frequencies f_i:

1. $f_i = f_o$;
2. f_i = the lowest frequency of the lock range (should be equal or very close to f_{min});
3. f_i = the highest frequency of the lock range (should be equal or very close to f_{max}).

In the report, compare the phase difference ϕ between v_i and v_{osc} to the theoretical prediction for the three frequencies of the incoming signal.

3.4 Characteristic of the PLL

Measure and sketch the characteristic $v_o(f_i)$ of the PLL. Note that v_o has a dc component with some high-frequency ac ripple around it. In this measurement we are interested in the dc component, which means that v_o can be measured using a dc voltmeter. Since f_{osc} is directly determined by v_o, this characteristic should have the same shape as the theoretical characteristic $f_{osc}(f_i)$ of Fig. 2. In particular, note the hysteresis in the characteristic, which means that you need to change f_i in both directions in order to obtain all parts of the characteristic correctly. During the measurement, it helps to monitor whether the PLL is locked or not. When the PLL is not in the locked condition, the voltage v_o should be equal to $V_{DD}/2$. Make sure that you determine the end points of the capture range and the lock range correctly. In your report, find a theoretical prediction for the $v_o(f_i)$ characteristic, and compare it to the measurement.

3.5 Effects of Changing the Loop Filter

In this part, you need to investigate effects of changing the cut-off frequency f_p of the loop filter on the capture range of the PLL and the high-frequency ripple in v_o. You can change f_p simply by changing one of the filter components (C_f or R_f). Cover the range $100Hz < f_p <$ 10kHz. Measure and plot, as functions of f_p:

1. The end points of the capture range, and the capture range $2f_c$;
2. The peak-to-peak ac ripple in the filter output voltage v_o, when the PLL is locked, and $f_i = f_o$.

In your report, compare the measured results with theoretical predictions.

Results of this lab assignment will be used for design purposes in the lab #5. Therefore, keep a copy of your report as a reference.

4 Prelab Assignment

The prelab assignment is due in the lab on the day when you start working on the experiment.

Note: Lab 4 is a **one-week** lab but you have two weeks to complete the report. See the due date on the Syllabus page.

Read the complete Lab 4 handout.

1. Select C_1, R_1, and R_2 in Fig. 3 of the handout, so that the VCO operates from $f_{min} = 8$kHz to $f_{max} = 12$kHz. Find the VCO frequency sensitivity K_o if the VCO characteristic $f_{osc}(v_o)$ is linear for $0 \leq v_o \leq V_{DD}$. The supply voltage is $V_{DD} = 15$V.

2. Select C_f and R_f so that the cut-off frequency of the low-pass filter is $f_p = 1$kHz.

3. Select C_i if the incoming signal frequency f_i is in the 5kHz to 15kHz range.

4. Assume that $v_i(t)$ is a square-wave signal at the frequency f_i, that the PLL is in the locked condition ($f_{osc} = f_i$), and that v_o is a dc voltage with negligible ac component. Sketch and label $v_i(t)$ and $v_{osc}(t)$, and determine voltage v_o, for:

   a) $f_i = 9$kHz

   b) $f_i = 10$kHz

   c) $f_i = 11$kHz

Make a copy of your prelab work so that you can use it during the Lab session.